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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/598,583
Filing Date: September 05, 2006
Appellant(s): BINK ET AL.

Robert J. Crawford, Reg. No 32,122
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2/18/2010 appealing from the Office action mailed 9/29/2009.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Hennessy et al. ("Computer Organization and Design: The Hardware/Software Interface", Morgan Kaufmann Publishers, 8-1997 2nd edition, pages 466-476) and Colwell et al. (U.S. 5,604,878, 2-1997) are relied upon as evidence.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Maintained Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hennessy et al. ("Computer Organization and Design: The Hardware/Software Interface"), in view of Colwell et al. (U.S. 5,604,878).

3. As per claim 1:

Hennessy and Colwell disclosed an electronic circuit adapted to process a plurality of types of instruction, the electronic circuit comprising:

first and second pipeline stages, each of the first and second pipeline stages generating pipeline data (Hennessy: Figure 6.25, pipeline stages MEM and WB)(The pipeline stages of the processor generate data.);

a latch positioned between the first and second pipeline stages (Hennessy: Figure 6.25, MEM/WB pipeline register)(Colwell: Figure 3 element 60, column 7 lines

13-15)(It's obvious to one of ordinary skill in the art that the pipeline register can be implemented as a latch. The pipeline extend buffer is the same as the MEM/WB pipeline register because it's output is written to the reorder buffer to finish execution. The output of the MEM/WB pipeline register writes to the register file to finish execution. Thus, in view of the combination, the pipeline extend buffer is equated to the MEM/WB pipeline register.); and

the electronic circuit is controlled by a control signal based on a latency period of each respective instruction of said plurality of types of instruction (Colwell: Figure 3 element 62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The combination uses elements 61-62 to bypass the MEM/WB pipeline register when a writeback contention will be avoided. The control logic outputs a control signal based on a latency period of an instruction being executed when writeback contention can be avoided.), said electronic circuit being controlled to operate in a normal mode when processing a first type of instruction in which the latch is opened and closed in response to an enable signal (Hennessy: Figures 6.32 and 6.33, load instruction)(The MEM/WB pipeline register is opened and closed by the inherent clock signal of the processor not shown, which is the enable signal.), and a reduced mode including a truncated passage when processing a second type of instruction in which the enable signal is overridden by the control signal so that the latch is held open for the generated pipeline data to propagate, independent of the enable signal through the latch. (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figures 6.26 and 6.33, subtraction instruction)(In Hennessy, say in

the first clock cycle a store instruction is issued, and in the second clock cycle a subtraction instruction (i.e. the second type of instruction) is issued. Looking at figure 6.33, in the fourth clock cycle, the store instruction writes its data back to data memory and the subtraction instruction is executing in the ALU. The store instruction at this point is finished and has no need for writing back to the register file in the fifth clock cycle. The subtraction instruction in the fifth clock cycle performs no action in the data memory stage because Hennessy forces all ALU type instructions to be extended by one clock cycle to avoid all potential writeback contentions to the register file. The subtraction instruction in the sixth clock cycle writes back to the register file. The combination uses the bypass control logic of Colwell to allow for the subtraction instruction to writeback in the fifth clock cycle, instead of the sixth clock cycle, as writeback contention is avoided on the register file due to the previous instruction being a store instruction. The recent KSR ruling supports that a claim would have been obvious because "a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely that the product is not of innovation but of ordinary skill and common sense." One of ordinary skill in the art would look at the Hennessy reference and realize that there are a finite number of ways for an ALU type instruction to bypass the MEM/WB pipeline register to allow for early retirement in the fifth clock cycle as detailed above. One of these ways would be to allow the MEM/WB pipeline register to be kept open during the fifth clock cycle as detailed above (i.e. the fourth executed clock cycle of the subtraction instruction), which allows for the ALU result to flow out of the MEM/WB pipeline register,

through the MUX, and be written into the register file during the fifth clock cycle as detailed above (i.e. the fourth executed clock cycle of the subtraction instruction). Thus, it would have been obvious to one of ordinary skill in the art to choose one of the finite number of solutions, i.e. keep the MEM/WB pipeline register open, to allow for the bypass teachings of Colwell to be implemented in Hennessy. Therefore, the combination reads upon the claimed limitations.); and

wherein the first type of instruction requires processing by the first and second pipeline stages (Hennessy: Figures 6.32 and 6.33, load instruction)(The load instruction requires processing by the MEM and WB stages.) and the second type of instruction requires processing by the second pipeline stage (Hennessy: Figure 6.33, sub instruction)(The subtraction instruction requires processing by the WB stage.).

The advantage of bypassing an extra pipeline stage that isn't needed for instructions is that these instructions will be allowed to retire earlier and result in increased performance when there is no writeback contention (Colwell: Column 2 lines 65-67 continued to column 3 lines 1-9). One of ordinary skill in the art would have been motivated to modify Hennessy to perform the pipeline stage bypassing of Colwell for the advantage above. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the pipeline stage bypassing of Colwell into the processor of Hennessy for the advantage of increasing performance of the processor of Hennessy.

4. As per claim 2:

Hennessy and Colwell disclosed the electronic circuit as claimed in claim 1, further comprising a latch control circuit connected to the latch, the latch control circuit configured to provide the enable signal to the latch to control the latch with the enable signal when the electronic circuit is in the normal mode (Hennessy: Figures 6.32 and 6.33, load instruction)(The MEM/WB pipeline register is opened and closed by the inherent clock signal of the processor not shown, which is the enable signal. The clock signal is part of the processor control unit.), and configured to hold the latch open by preventing the enable signal from being provided to the latch when the electronic circuit is in the reduced mode (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The recent KSR ruling supports that a claim would have been obvious because "a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely that the product is not of innovation but of ordinary skill and common sense." One of ordinary skill in the art would look at the Hennessy reference and realize that there are a finite number of ways for a ALU type instruction to bypass the MEM/WB pipeline register to allow for early retirement in the fourth clock cycle of the instruction. One of these ways would be to allow the MEM/WB pipeline register to be kept open during the fourth clock cycle of the ALU type instruction, which allows for the ALU result to flow out of the MEM/WB pipeline register, through the MUX, and be written into the register file during the fourth clock cycle. Thus, it would have been obvious to one of ordinary skill in the art to choose one of the finite number of solutions, i.e. keep the MEM/WB pipeline register

open, to allow for the bypassing teachings of Colwell to be implemented in Hennessy. Therefore, the combination reads upon the claimed limitation.).

5. As per claim 3:

Hennessy and Colwell disclosed the electronic circuit as claimed in claim 2, wherein the latch control circuit receives the control signal indicating whether the electronic circuit operates in the normal mode or in the reduced mode (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(The control logic generates a signal that determines the mode of the processor when Hennessy is acting as a 4 or 5 stage pipeline.).

6. As per claim 4:

Hennessy and Colwell disclosed the electronic circuit as claimed in claim 1, wherein the electronic circuit is adapted to process a third type of instruction, wherein the third type of instruction does not require processing by the second pipeline stage (Hennessy: Figures 6.26 and 6.28, pages 466 and 468, store and branch instructions)(Store and branch instructions don't write to the register file, which is the second pipeline stage, as shown by the control signals in figure 6.28.).

7. As per claim 5:

Hennessy and Colwell disclosed the electronic circuit as claimed in 4, wherein the electronic circuit is adapted to operate in the normal mode until an instruction of the third type of instruction is processed (Hennessy: Figures 6.31-6.34)(The processor acts in a normal mode of processing where instructions are processing in 5 stages.).

8. As per claim 6:

Hennessy and Colwell disclosed the electronic circuit as claimed in claim 5, wherein, after the instruction of the third type of instruction is processed, the electronic circuit is adapted to operate in the reduced mode if an instruction, following the instruction of the third type of instruction, is of the second type of instruction or the third type of instruction (Hennessy: Figure 6.26, page 466 and 468, store and branch instructions)(Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(When a store instruction is processed, it doesn't write to the register file in the fifth stage, which allows a preceding instruction to write to the register file in the fourth pipeline stage by utilizing the bypass of Colwell. This results in changing the processor to a reducing mode. It's inherent that the bypass can not be utilized if the preceding instruction is a load instruction that must write to the register file in the fifth pipeline stage in the pipelined processor of Hennessy that issued a single instruction per cycle and has a single writeback port on the register file.).

9. As per claim 7:

Hennessy and Colwell disclosed the electronic circuit as claimed in claim 4, wherein the electronic circuit is adapted to operate in the reduced mode until an instruction of the first type of instruction is processed (Hennessy: Figure 6.26, page 466 and 468, store and branch instructions)(Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(When a store instruction is processed, it doesn't write to the register file in the fifth stage, which allows a preceding instruction to write to the register file in the fourth pipeline stage by utilizing the bypass of Colwell. This results in changing the processor to a reducing mode. It's inherent that the bypass

can be utilized until a load instruction is executed, which must write to the register file in the fifth pipeline stage.).

10. As per claim 8:

Hennessy and Colwell disclosed the electronic circuit as claimed in claim 1, wherein the first type of instruction includes a load instruction (Hennessy: Figure 6.26)(The load instruction is the first type of instruction.), and wherein the first and second pipeline stages are asynchronous pipeline stages that are each controlled responsive to different enable signals (Official notice is given that processors can be implemented as asynchronous processors. Thus, the processor of Hennessy can be implemented as an asynchronous processor. An asynchronous processor is controlled by signals to allow for processing to continue to a next stage at the time when a next stage is ready for the data.).

11. As per claim 9:

Hennessy and Colwell disclosed the electronic circuit as claimed in claim I, wherein the second type of instruction includes an arithmetic computation instruction (Hennessy: Figure 6.26)(The add and sub instructions are the second type of instructions.).

12. As per claim 10:

Hennessy and Colwell disclosed the electronic circuit as claimed in claim 4, wherein the third type of instruction includes compare, store, branch and jump instructions (Hennessy: Figure 6.26)(The store and branch instructions are the third type of instructions. Official notice is given that jump and compare instructions don't

write results to the register file. Thus, it's obvious to one of ordinary skill in the art to include jump and compare instructions in the processor of Hennessy as the third type of instructions.).

13. As per claim 11:

Hennessy and Colwell disclosed the electronic circuit as claimed in claim 1, wherein the first pipeline stage comprises a data memory (Hennessy: Figure 6.25, MEM pipeline stage.).

14. As per claim 12:

Hennessy and Colwell disclosed the electronic circuit as claimed in any claim 1, wherein the second pipeline stage comprises a write back stage (Hennessy: Figure 6.25, WB pipeline stage.).

15. As per claim 13:

Claim 13 essentially recites the same limitations of claim 1. Therefore, claim 13 is rejected for the same reasons as claim 1.

16. As per claim 14:

The additional limitation(s) of claim 14 basically recite the additional limitation(s) of claim 4. Therefore, claim 14 is rejected for the same reason(s) as claim 4.

17. As per claim 15:

The additional limitation(s) of claim 15 basically recite the additional limitation(s) of claim 5. Therefore, claim 15 is rejected for the same reason(s) as claim 5.

18. As per claim 16:

The additional limitation(s) of claim 16 basically recite the additional limitation(s) of claim 6. Therefore, claim 16 is rejected for the same reason(s) as claim 6.

19. As per claim 17:

The additional limitation(s) of claim 17 basically recite the additional limitation(s) of claim 7. Therefore, claim 17 is rejected for the same reason(s) as claim 7.

20. As per claim 18:

The additional limitation(s) of claim 18 basically recite the additional limitation(s) of claims 2 and 8. Therefore, claim 18 is rejected for the same reason(s) as claims 2 and 8.

21. As per claim 19:

The additional limitation(s) of claim 19 basically recite the additional limitation(s) of claims 8-9. Therefore, claim 19 is rejected for the same reason(s) as claims 8-9.

22. As per claim 20:

The additional limitation(s) of claim 20 basically recite the additional limitation(s) of claim 10. Therefore, claim 20 is rejected for the same reason(s) as claim 10.

(10) Response to Argument

23. Regarding claims 1-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hennessy et al. ("Computer Organization and Design: The Hardware/Software Interface"), in view of Colwell et al. (U.S. 5,604,878):

A.) Appellant argues "For example, the '878 reference teaches bypassing a pipe extend buffer 60 in a manner that does not involve data propagating through the buffer

60. *See, e.g.,*Figure 3 and Col. 7:55-62. Instead, the data is routed without passing through the buffer 60 as is shown in Figure 3. As such, the Examiner fails to cite to any reference that teaches that a latch is held open for the generated pipeline data to propagate through the latch in the reduced mode, as claimed … Appellant further submits that the Examiner is improperly attempting to modify the Hennessy reference in a manner that is taught, not by the cited references, but by Appellant, in a blatantly improper hindsight reconstruction of the claimed invention using Appellant's disclosure as a template. *See, e.g.,* M.P.E.P. § 2142" for claim 1.

The examiner disagrees for the following reasons. While the examiner agrees that the "reduced mode" limitation isn't explicitly taught by Colwell, the combination of Hennessy, Colwell, and the reasoning from recent KSR ruling are used to properly reject the claimed limitation. The examiner gives an example of an instruction sequence and how the bypassing control logic of Colwell is implemented by the combination. In Hennessy, say in the first clock cycle a store instruction is issued, and in the second clock cycle a subtraction instruction (i.e. the second type of instruction) is issued. Looking at figure 6.33, in the fourth clock cycle, the store instruction writes its data back to data memory and the subtraction instruction is executing in the ALU. The store instruction at this point is finished and has no need for writing back to the register file in the fifth clock cycle. The subtraction instruction in the fifth clock cycle performs no action in the data memory stage because Hennessy forces all ALU type instructions to be extended by one clock cycle to avoid all potential writeback contentions to the register file. The subtraction instruction in the sixth clock cycle writes back to the

register file. The combination uses the bypass control logic of Colwell to allow for the subtraction instruction to writeback in the fifth clock cycle, instead of the sixth clock cycle, as writeback contention is avoided on the register file due to the previous instruction being a store instruction. The recent KSR ruling supports that a claim would have been obvious because "a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely that the product is not of innovation but of ordinary skill and common sense." One of ordinary skill in the art would look at the Hennessy reference and realize that there are a finite number of ways for an ALU type instruction to bypass the MEM/WB pipeline register to allow for early retirement in the fifth clock cycle as detailed above. One of these ways would be to allow the MEM/WB pipeline register to be kept open during the fifth clock cycle as detailed above (i.e. the fourth executed clock cycle of the subtraction instruction), which allows for the ALU result to flow out of the MEM/WB pipeline register, through the MUX, and be written into the register file during the fifth clock cycle as detailed above (i.e. the fourth executed clock cycle of the subtraction instruction). Thus, it would have been obvious to one of ordinary skill in the art to choose one of the finite number of solutions, i.e. keep the MEM/WB pipeline register open, to allow for the bypass teachings of Colwell to be implemented in Hennessy. Therefore, the combination reads upon the claimed limitations.

B.) Appellant argues "Instead, the '878 reference teaches that a pipe extend buffer 60 is added after the end of the third pipe stage 43 of the unit. *See, e.g.,* Figure 3. The '878 reference uses the buffer 60 to extend the length of the pipeline when

writeback conflict exists. *See, e.g.,* Col. 7:55-66. As such, the '878 reference teaches a normal mode and an extended mode, and the '878 reference fails to teach a reduced mode of operation, which involves such a latch being held open for pipeline processing as claimed. The Examiner generally and without explanation or supporting rationale asserts that the ' 878 reference teaches a reduced mode of operation, but no such mode is taught by the '878 reference as discussed above" for claim 1.

The examiner disagrees for the following reasons. If one was to look solely at Colwell without any view of the combination, one would apply the output of the pipe extended buffer being selected as operating in the normal mode and the output of element 43 bypassing the pipe extend buffer being selected as operating in the reduced mode. The combination, in view of KSR, as disclosed above, taught the reduced mode that allows for the MEM/WB pipeline register of Hennessy to be held open in certain instruction sequences when writeback contention (i.e. two writes to the register file at once when only one write is allowed) to the register file is avoided according to control logic element 62.

C.) Appellant argues "Appellant submits that Hennessy further does not teach a latch control circuit that prevents the enable signal from being provided to the latch in an apparently nonexistent reduced mode. The '878 reference also fails to teach such aspects of the claimed invention. For example, the '878 reference does not teach that control logic 60 *(i.e.,* the asserted latch control circuit) provides any signals to buffer 60. Instead, the control logic 62 provides a control signal to MUX 61 to select the desired output. *See, e.g.,* Figure 3. As such, the control logic 60 of the '878 reference does not

provide an enable signal, or prevent the enable signal from being provided, to a pipeline stage *(e.g.,* the claimed latch)" for claim 2.

The examiner disagrees for the following reasons. In view of the above combination, the MEM/WB pipeline register is allowed to be held open when it would otherwise normally be held closed. Inherently, a clock signal (i.e. the enable signal) is used to control the timing of the closing and opening of the pipeline stages to synchronize the processor as to when data can pass from one stage to another. The combination allows for the overriding of this clock signal to hold open the MEM/WB pipeline register when it would otherwise be normally closed. Thus, inherently, the combination includes logic to override the clock signal from normally being applied to the MEM/WB pipeline register to close the register and prevent data being passed to the next stage.

D.) Appellant argues "However, Appellant submits that bypassing the MEM/WB stage (asserted by the Examiner to be a latch) would result in the corruption of the data being processed by Hennessy's synchronous pipeline processor. Specifically, bypassing the MEM/WB stage would result in the data output by the pipeline stage prior to the MEM/WB stage being passed through the MEM/WB stage to the pipeline stage after the MEM/WB stage prior to the receipt of the next pulse of the clock signal. As such, the input data to the pipeline stage after the MEM/WB stage would change before that stage finishes processing the current data, thereby resulting in the corruption of data being processed by the pipeline stage after the MEM/WB stage."

The examiner disagrees for the following reasons. The examiner gave an example in “Argument A” above that directly refutes the appellants claims. Any ALU instruction following a store instruction in Hennessy is needlessly delayed by a clock cycle from writing to the register file for simplicities sake in ensuring that no writeback contentions occur (i.e. two writes to the register file when only one is allowed.). The combination uses the control logic of Colwell to ensure that no corruption occurs.

E.) Appellant argues “Specifically, the Examiner erroneously asserts that "(w)hen the ALU instruction reaches the fourth pipeline stage, the control logic of Colwell [the ' 878 reference] determines that no conflict occurs in the fifth pipeline stage and that the ALU instruction can wire its data a clock cycle early to the register file" *(see* page 11 of the Final Office Action dated September 29, 2009). The '878 reference, however, does not teach that the control logic 62 allows for bypassing pipeline stages in the middle of Hennessey's synchronous pipeline processor. Instead, the '878 reference teaches that a pipe extend buffer 60 is added after the end of the third pipe stage 43 of the unit to extend the pipeline. *See, e.g.,* Figure 3. The '878 reference uses the buffer 60 and the control logic 62 to extend the length of the pipeline when writeback conflict exists.”

The examiner disagrees for the following reasons. The appellant seems to be missing the fact that the pipe extend buffer that extends a pipeline stage for Fadd instructions is the exact same method of Hennessy extending the pipeline by a stage for ALU type instructions by adding the MEM/WB pipeline register. Hennessy shows that ALU type instructions perform no action in the MEM stage and are extended by one

clock cycle in the same way that Colwell extends the Fadd instruction by one clock cycle. The only difference between the two references is that Hennessy uses the MEM/WB pipeline register to **extend every ALU type instruction** due to assuming writeback contention with the previous instruction and that Colwell uses the bypass logic to **selectively extend Fadd type instructions** (emphasis added). Therefore, the references teach the exact same thing in regards to extending the pipeline length of certain instructions to avoid writeback contention.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Jacob Petranek/

/JAP/

March 31, 2010

Conferees:

Eddie Chan

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